UNITED STATES PATENT AND TRADEMARK OFFICE

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10/002,461	11/01/2001	Keith R. Slavin	DB000955-000	5286

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ART UNIT	PAPER NUMBER
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)
Office Action Summary		10/002,461	SLAVIN, KEITH R.
		Examiner	Art Unit	
		Reba I. Elmore	2189	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>20 September 2007</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38 and 41-44* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38 and 41-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>01 November 2001</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-38 and 41-44 are presented for examination. Claims 39 and 40 have been

cancelled.

2.   The granting of the petition under 37 CFR 1.183 is acknowledged.

3.   The affidavit or declaration filed on April 6, 2007 under 37 CFR 1.131 is sufficient to

overcome the Allen et al. (P/N 6,538,911) reference.

DRAWINGS

4.   The drawings are objected to because labels need to be added for elements 28 and 38 of

Figure 1, element 40(1) of Figure 2 and elements 50(1), 56, 58 and 60 of Figure 3.

5.   Figure 6 should be designated by a legend such as --Prior Art-- because only that which is

old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR

1.121(d) are required in reply to the Office action to avoid abandonment of the application. The

replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR

1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted

by the examiner, the applicant will be notified and informed of any required corrective action in

the next Office action. The objection to the drawings will not be held in abeyance.

6.   Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to

the Office action to avoid abandonment of the application. Any amended replacement drawing

sheet should include all of the figures appearing on the immediate prior version of the sheet,

even if only one figure is being amended. The figure or figure number of an amended drawing

should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

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must be removed from the replacement sheet, and where necessary, the remaining figures must

be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The

objection to the drawings will not be held in abeyance.

SPECIFICATION

7.   The abstract of the disclosure is objected to because the submitted abstract contains

language which is not recommended for the content of the abstract and also contains a sentence

which appears to be directed to a different invention than the presently claimed invention.

Correction is required. See MPEP § 608.01(b).

8.   The following abstract will be printed unless the Applicant provides a new abstract.

> *A comparand word is input to a plurality of hash circuits with each hash circuit*
>
> *responding to a different portion of the comparand word. The hash circuit outputs a*
>
> *hash signal which enables or pre-charges portions of a content addressable memory*
>
> *(CAM). The comparand word is also input to the CAM. The CAM compares the*
>
> *comparand word in the pre-charged portions of the CAM and outputs information*
>
> *responsive to the comparison. When Internet addresses are processed, the output*
>
> *information is either port information or an index for locating port information.*

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9.   The specification has not been checked to the extent necessary to determine the presence

of all possible minor errors. Applicant's cooperation is requested in correcting any errors of

which applicant may become aware in the specification. .

35 USC 112, 1st Paragraph

10.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making
> and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it
> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
> contemplated by the inventor of carrying out his invention.

11.   Claims 1-38 and 41-44 are rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The claim(s) contains subject matter which

was not described in the specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventor(s), at the time the application was filed, had possession of the

claimed invention.

12.   Delaying the input of the comparand word to the CAM has been claimed in claims 4, 11,

17, 24 and 34. A delay circuit is shown in Figures 1 and 5, elements 28 and 114, respectively,

however, nothing more than a blank box or a black box type design is depicted which fails to

give any details for one of ordinary skill in the memory arts to make and use a delay circuit in

conjunction with a content addressable memory without undue experimentation. The delay

circuit is mentioned on page 4, paragraph 0019 and page 14, paragraph 0057 of the specification

without providing sufficient technical details for essential subject matter. The claims state that

the input word or comparand word is delayed in being input to the CAM until the enabling is

completed, however, nothing is given which describes how a delay of the input is to be

determined or what parameters must be met for a 'delay circuit' to be used. How does the

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determination of the enabling get performed and how is that determination used to notify the

delay circuitry for the comparand word to be input to the CAM.

13.   The written description persistently uses non-descriptive, non-specific language, for

instance, 'may be implemented', 'may be stored' with language being used 'This invention is not

limited to any particular way of implementing hash logic 40(1).' or 'The manner in which the

hash output signal is used to identify, enable and/or precharge portions of the TACM 20 is not an

important future *(feature?)* of the present invention.' 'Accordingly, although the present

preferred method of using the hash output signal to identify, enable, and/or precharge portions of

TCAM 20 will now be described, the present invention is not to be limited by the presently

preferred embodiment.' The specification does not state how the invention is *actually* made,

what elements or steps are *actually* used or implemented or how elements or steps *actually*

interact for the present invention. The law requires that the written description be clear and

precise as to how the Applicant performs such activities as those claimed. If memory elements

are not limited as to which types can be used and steps or instructions are not limited as to what

step or instruction is performed, where is the inventiveness of the present invention? The

novelty of the present invention must be disclosed in such detail as to allow one of ordinary skill

in the art to make and use the invention without undue experimentation. Such details for the

actual inventive concepts have not been given in the present disclosure. Legal support for these

reasons for a determination that the written disclosure is not adequate can be found in the recent

US Court of Appeals for the Federal Circuit, Automotive Technologies International, Inc., v.

BMS of North America, Inc ... (2006-1013,-1037).

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35 USC § 102

14.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United
States before the invention thereof by the applicant for patent, or on an international application by another who
has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention
thereof by the applicant for patent.

15.   Claims 41-44 are rejected under 35 USC 102(e) as being anticipated by Cheriton (P/N

7,002,965).

16.   Cheriton teaches the invention (claim 41) as claimed including a method of initializing

hardware, the method comprising:

transferring network address to a CAM based on an index to a hash table (e.g., see col. 6,

lines 8-25);

transferring port numbers to an output memory device responsive to the CAM (e.g., see

col. 3, lines 12-42);

modifying bit prefix values to obtain a ternary representation (e.g., see col. 4, lines 27-

42);

calculating bank run length information as packet information (e.g., see col. 6, lines 43-

49); and,

loading starting address and bank run length information into a plurality of memory

devices as packet information including IP source and destination addresses, protocol type

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information as well as other data associated with the packets (e.g., see col. 6, line 43 to col. 7, line 21).

As to claim 42, Cheriton teaches periodically transferring invalid addresses to the CAM as specialized rules which allow restrictive protocols of the TCAM (e.g., see col. 4, lines 43-60).

As to claim 43, Cheriton teaches transferring port information to an SRAM for prefixes below a certain length (e.g., see col. 3, lines 12-42).

17.   As to claim 44, Cheriton teaches bank run length information includes one of an end address and an address span as packet information (e.g., see col. 6, line 43 to col. 7, line 21).

35 USC § 103

18.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19.   Claims 1-38 are rejected under 35 USC 103(a) as being unpatentable over Hariguchi et al. (P/N 6,665,297) in view of Cheriton (P/N 7,002,965).

20.   Hariguchi teaches the invention (claims 1, 8, 15, 22, 28 and 34) as claimed including a method or circuit, the method or circuit comprising:

inputting an input word or comparand word with the word being Internet addresses which have different prefixes or indexes to a plurality of hash circuits, each hash circuit being responsive to a different portion of the input word as there being different hash circuits which are used dependent upon the prefix length with each hash circuit determining a match based upon a

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predetermined portion of the address (e.g., see Figures 2A-2B with support at col. 1, lines 23-50

and col. 5, lines 15-31);

outputting a hash signal from each hash circuit as each hash circuit (e.g., see elements *82-*

n of Figure 2A) having an output to the selection stage (e.g., see element 88 of Figure 2A);

enabling or precharging portions of a CAM in response to the hash signals as portions of

the CAM being enabled when the hash signals indicating the CAM has a match of the prefix

(e.g., see col. 7, line 50 to col. 8, line 3);

inputting the input word or comparand word to the CAM as inputting the IP destination

address to the hash circuits and the CAM (e.g., see Figure 7, step 204);

comparing the Internet address in the CAM as identifying a hit from the comparison of

the IP destination address and the contents of the CAM (e.g., see Figure 7);

outputting information responsive to the comparing of the IP destination address from

either the hash circuits of the CAM (e.g., see Figure 7, steps 208 and 210);

a plurality of memory devices responsive to the hash circuits as hash buckets which

respond to the entries of the hash stages and look-up tables (e.g., see Figures 2A-2B with support

at col. 5, lines 15-63);

enable logic, responsive to the plurality of memory devices, for enabling portions of the

CAM as being inherent as the CAM must have enable logic; and,

a delay circuit for inputting the comparand word or Internet address as stages of a

pipeline with the hash circuit having two pipeline stages which means the hash bucket stage is at

a later stage or is delayed according to clock cycles from the first stage or hash stage (e.g., see

col. 5, lines 15-31).

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Hariguchi teaches the limitations of the independent claims as given above, however, the

primary reference does not specifically teach using hash signals to enable portions of a CAM.

Cheriton (P/N 7,002,965), the secondary reference teaches using a hash function to enable or

choose portions of a CAM as generating classification indications which allows for packet

classification in network routers (e.g., see Figure 3 with support at col. 6, line 43 to col. 7, line

21). It would have been obvious to one of ordinary skill in the memory arts at the time the

invention was made to use hashing to select addresses in a CAM because using a CAM (or a

TCAM) as a routing table or directory is a well known and common use of content addressable

memories (e.g., see the background of Cheriton) and using hashing functionality for determining

addresses for Internet address routing and address port information is also a common, well

known type of addressing. The combination of adding hash type addressing to using CAMs or

TCAMs for routing data provides for a fast, methodical and reasonable use of current

technology.

As to claims 2, 9, and 16, Hariguchi teaches assigning a mask to each hash circuit such

that each hash circuit is responsive to a different n-bit portion of the input word or comparand

word as different n-bit portions of the IP destination address being an associated prefix length of

a predetermined portion of the address (e.g., see col. 5, lines 15-31).

As to claims 3, 10, 17 and 23, Hariguchi teaches inputting the least significant n bits of

the input word or IP destination address to a memory and wherein the outputting selects between

information responsive to finding a match of the address being found in the look-up tables or

memory associated with the different hash circuits and the CAM (e.g., see Figure 2B with

support at col. 5, lines 50-63).

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As to claims 4, 11, 18 and 24, Hariguchi teaches delaying the inputting of the input word

or comparand word to the CAM until the enabling or precharging is completed as part of the

router control procedure which is stored in the memory for controlling the overall operation of

the router (e.g., see col. 4, lines 31-62).

As to claims 5, 12, 19 and 25, Hariguchi teaches enabling includes using the hash signals

to select from a plurality of stored signals and using the selected stored signals to enable or

precharge a portion of the CAM (e.g., see col. 4, line 63 to col. 5, line14).

As to claims 6-7, 13-14, 20-21 and 26-27, Hariguchi does not specifically teach the

stored signals include using a run length or ending index in conjunction with a starting index,

however, the reference does teach using a starting index to help select a network destination for

the sending of a datagram. Sending a datagram means the length of the data to be sent must also

be specified or known which indicates using either a run length or an ending index for the

determination of a message length because the purpose of the invention as taught by Hariguchi is

to select an Internet address for sending a datagram or message which means sending not only

the address information but also sending the length of the datagram whether the length is

conveyed as a run length or as an ending index.

As to claim 29, Hariguchi teaches the circuit is responsive to the hash signals includes a

plurality of memory devices respond to the hash signals and enable logic for the plurality of

memories with the memories being buffers, tables, registers and the CAM (e.g., see Figures 2A-

2B).

As to claims 30 and 35, Hariguchi does not specifically teach using SRAMs for portions

of the memory, however, the reference does teach using semiconductor memory including

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random access memory. Cheriton teaches using on-chip SRAM for the hash directory (e.g., see col. 6, lines 43-65). It would have been obvious to one of ordinary skill in the memory arts to combine the teachings of Cheriton with the teachings of Hariguchi because both references use hash tables in the same manner with both references using semiconductor memory for this function. The present invention does not further define using SRAM for the hash circuitry over any other type of random access memory, therefore making it obvious to use SRAM as given in the secondary reference.

As to claims 31 and 36, Hariguchi teaches an output memory devices responsive to the CAM for outputting information in response to a match in the CAM as the selection stage (e.g., see Figure 2B with support at col. 5, lines 50-63).

As to claims 32 and 37, Hariguchi teaches an input memory device responsive to a portion of the comparand word and a switch responsive to the input memory device and the output memory device with the switch being inherent as part of the circuitry for the selection stage (e.g., see Figures 2A-2B).

As to claims 33 and 38, Hariguchi teaches having a processor (e.g., see Figures 2A-2B, element 54), the plurality of hash circuits as hash table having hash circuits with hash stages and hash bucket stages (e.g., see Figures 2A-2B, element 70) with the circuit response to the hash circuits receiving information from the processor (e.g., see Figures 2A-2B) as the information from the processor including router control procedures which uses the routing table (e.g., see Figures 2A-2B). Figure 4 also shows data and addresses from the CPU being input to the hash circuit and the hash bucket circuitry.

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RESPONSE TO APPLICANT'S REMARKS

21.   Applicant's arguments with respect to claims 1-38 and 41-44 have been considered but are moot in view of the new ground(s) of rejection.

CONCLUSION

22.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Monday and Thursday from 7:30am to 6:00pm, EST.

     If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

     Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2189

Wednesday, November 28, 2007

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